1. Claims 1-5,7-57,59-80,82-88,115,116,118-121, 123-128,144,145 are presented for examination. Claims 6,58,81,89-114,117, 122, 129-143 have been canceled. TD. on 12/04/06 on 6,986,021 has been received. IDS 1449 on 11/05/07 has not been received. The cover of IDS on 11/05/07 is on the record, but no 1449 form has been recieved.

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel,422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 7,320,062. Although the conflicting claims are not identical, they are not patentably distinct from each other because although current claim 1 did not specifically show the first routable and executable information module having the first configuration and having the routing sequence as claimed in the co-pending claim 1, the current claim 1 disclosed configuration information and the plurality of routing elements adapted to provide a selected operating mode by selectively selecting data and the configuration information (see current claim 1, lines 9-12), which was recognizable by one of ordinary skill in the art that the plurality of routing elements were would also applicable for routing sequence for the purpose of selecting the operating mode for routing of the selected data.

4. Claims 1, 9, 10, 11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

5. As to claims 1, 9, 10, 11, claims 1, 9, 10,11are not limited to tangible embodiments. In view of Applicant's disclosure, specification page 7 , lines 1-3,15,31, the system for adaptive configuration is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., [wireless base station]) and intangible embodiments (e.g., [wireless link] [air interface]). See also page 9. line 31 [wireless interface], page 27, line 10 [download through other medium], page 27,

lines 29,30 [wireless download]. No clear adaptive configuration system can be found. As such, the claim is not limited to statutory subject matter and is therefore non-statutory. The invention is not restricted into the hardware. For example, routing of the first subset configuration information and the routing of the data through the interconnect network could be done over the air interface, for example the wireless download; therefore, it is not concrete and tangible. The first subset of configuration information is non-functional descriptive material. The downloaded configuration information can be in the form of frequency waves transmitted in the air space or the wireless download, therefore, it is directed to a non-statutory subject matter. No specific type of interconnection network and the computational elements are being reflected into the claims. Therefore, interconnection network and the computational elements are read as a general arrangement of the functional parts.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,7-15, 17, 18, 20,21,23,27-31, 115-128, 144,145 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Brewer (5,519, 694).

As to claims 1,8,17, Wise taught system for adaptive configuration, the system comprising:

a first set of configuration information (see fig.137) comprising a first subset of configuration information (see carry-save multiplier , carry save adder, carry save subtractor) and a second subset of configuration information (carry-save multiplier , carry save subtractor, carry save subtractor);

a first plurality of fixed and differing computational elements (see resolving adder at y input) ; a second plurality of fixed and differing computational elements(see the d multiplier at x, see the adder different form the multiplier) ;

an interconnection network coupled to the first and second pluralities of computational elements (see common block in fig.137), comprising:

a plurality of routing elements (see input and output connections x y in fig.137) adapted to provide a selected operating mode of a plurality of operating modes x[3,4] x[2,5] by selectively routing data and the first and second subsets of configuration information to the corresponding first or second pluralities of computational elements (see configuration carry-save multiplier, carry save adder, carry save subtractor in the common block) and

a second level of the interconnection network comprising a plurality of switching elements (see multiplexer circuit in fig.137) adapted to configure the first plurality of computational elements for a first functional mode x[3,4] of a plurality of functional modes in response to the first subset of configuration information (see the input selection), and to configure the second plurality of computational elements for a second, different functional mode of the plurality of functional modes x[3,4] x[2,5] , in response to the second subset of configuration information (see carry save multiplier, carry save subtractor, carry save subtractor in the configurable circuit in fig.137).

Wise did not specifically show the first level and the second level as claimed. However, Brewer taught a switching network included multiple levels of routers or switches (see multistage routers in col.2, lines 14-27, col.8, lines 19-38 for two level hierarchy routers, see also col1. lines 5-15 for background teaching of the routers and switches). It would have been obvious to one of ordinary skill in the art to use Brewer in Wise for including the first level and second level as claimed because the use of Brewer could provide Wise the ability to include deeper levels of interconnection network , thereby expanding the system interconnectivities, and because Wise also taught a memory map for mapping hardware resources into the memory address (see col.259, lines 10-25), and that his multiplexed network (see interconnection common box in fig.137) showed the points at which needed to be stored (see col.262, lines 14-20), which was recognizable by one of ordinary skill in the art that Wise's mapping of hardware

resources were applicable for multilevel of the interconnect for purpose of higher level of network multiplexing.

As to claim 2, Wise also taught the first set of configuration information provides a first system operating mode of the plurality of operating modes (see carry-save multiplier , carry save adder, carry save subtractor).

As to claim 3, Wise also taught store a second set of configuration information, the second set of configuration information providing a second system operating mode Of the plurality of operating modes (carry-save multiplier , carry save subtractor, carry save subtractor).

As to claim 4, the first set of configuration information corresponds to a first system configuration capacity and the second set of configuration information corresponds to a second system configuration capacity (see the y[3,2] x[3,4] connection path in fig.137, see a second system configuration capacity y[7,6] , x[2,5]) .

As to claim 5, selected from a plurality of sets of configuration information (see fig.137).

As to claim 7, Wise also taught a second plurality of computational elements configured for a memory functional mode (see the RAM organized into common control block in col.265, lines 43-53, see also the common control block in fig.137).

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As to claim 8, comprises a configuration of the plurality of computational elements in response to the first set of configuration information (see carry-save multiplier , carry save adder, carry save subtractor).

As to claim 9, the first set of configuration information is transferred to the system from a machine-readable medium (see microprocessor read port in col.260, lines 32-35, see RAM in col.265, lines 43-53).

As to claim 10,11 the first set of configuration information is transmitted to the system through a wireless interface.

As to claims 12,13, Wise also taught the first set of configuration information is embodied as a stream of information data bits and a first set of configuration information is embodied as a plurality of discrete information data packets (see Discrete cosine transform in col.4, lines 1-11 for background, see also the data packet in col.13, lines 53-57).

As to claim 14, Wise further taught a plurality of fixed circuit architectures to perform at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, Output, and field programmability (see memory, addition (see adder) , multiplication (see multiplier) , complex multiplication , subtraction (see subtractor) , configuration,

reconfiguration, control, input, output (input and output and field programmability in dynamic adaptive configuration in col.6, lines 57-67, col.7, lines 1-12).

As to claim 15, Wise also included linear algorithmic operations (see col.4, lines 8-9), non-linear algorithmic operations (see the transforms), finite state machine operations (see state machine stages in col.30, lines 62-67, col.31, lines 1-4), controller operations, memory operations (see col.39, lines 35-57), and bit-level manipulations (see bit operation in col.40, lines 15-28).

As to claim 18, Wise was also taught time and schedule the configuration of the first and second pluralities of computational elements with corresponding data (see the pipeline control of the algorithm and the control clock signals in col.262, lines 55-65).

As to claim 20, Wise also configured for a controller functional mode of the plurality of functional modes, the second plurality of computational elements is adapted to direct and schedule the configuration of the first plurality of computational elements for the first functional modes (see the clock control circuit at input in fig.141, see also the pipeline control of the algorithm and the control clock signals in col.262, lines 55-65)).

As to claim 21, Wise also included a second plurality of computational elements is further adapted to time and schedule the configuration and reconfiguration of the

plurality of heterogeneous computational elements with corresponding data (see fig.141 the output clock latches).

As to claim 23, Wise did not explicitly show the mobile station having a plurality of operating modes. However, Wise in the background taught carrier waves by a transmitter (see carrier waves, see col.4, lines 21-23). Therefore, Wise must have included a mobile station.

As to claim 27, Wise also taught request for configuration information (see the request in col.64, lines 34-50).

As to claims 28,29, 30, Wise also determined system reconfiguration capacity prior to utilizing the second set of configuration information to reconfigure for a second system operating mode (see the token information for reconfiguration in col.61, lines 5-22, see also the prediction filters to perform either filtering based on the token fig.17, col.69, lines 11-20).

As to claim 31, Wise also taught a first portion of the plurality of computational elements (see configuration carry-save multiplier , carry save adder, carry save subtractor in the common block) are operating in the first functional mode (x[3,4]) while a second portion of the plurality of computational elements (see carry save

multiplier, carry save subtractor, carry save subtractor) are being configured for the second functional mode (x[2,5]).

As to claim 115, Wise's also included computational element which is different than the computational elements comprising the first plurality of computational elements (see carry save adder is different from carry save subtractor).

As to claim 116, Wise also independently configure the first plurality of computational elements and the second plurality of computational elements (see each connection path in fig.137).

As to claims 118, 119, Wise also selectively switched his data to the plurality of computational elements (see multiplexed circuit in fig.137).

As to claims 120, 121, Wise's intercconection network also provided a third mode (see the arithmetical functional modes set forth in the fig.137, see a third path at x input, see multiplexed circuit for selectively switching).

As to claims 125,126, Wise also taught all limitations in claim 1 as set forth above, and further included the interface circuit (see the input at X and output at y in fiog.137). As to the selectively switch, see multiplexed circuit in fig.137), and selectively routing.

As to claim 127, see multiplexers in fig.137.

As to the demultiplxers in clam 128, since no specific type of demultiplexers are being reflected into the claim, therefore, examiner holds that demultiplexers were already well known in the art.

As to new claim 144, examiner holds that memory for holding configuration information had been known in the art unless applicant can show unique type of memory and unique type of configuration.

As to new claim 145, examiner holds that single chip with fixed and differing elements had been known in the art unless applicant can show unique type of single chip.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 123, 124 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Brewer (5,519, 694) as applied to claim 1 above, and further in view of Baxter (5,794,062).

7. As to claims 123, 124, neither Wise nor Brewer specifically showed the self-routing as claimed. However, Baxter included a self-routing (see the reconfigurable information stored in the memory by the directives in fig.2). It would have been obvious to one of ordinary skill in the art to use Baxter for including the self-routing as claimed because Wise also taught the determination of system reconfiguration capacity prior to utilizing the second set of configuration information to reconfigure for a second system operating mode (see the token information for reconfiguration in col.61, lines 5-22, see also the prediction filters to perform either filtering based on the token fig.17, col.69, lines 11-20)., and therefore suggested the need for self-routing, such as the reconfigurable information, or the like.

8. Claims 32-46, 48,49, 51-57, 60, 62-80, 82-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Brewer (5,519, 694) and Baxter (5,794,062).

9. As to claims 32,46, 48,49,51-57, 60, 62-76, 78-80, 82-85,87, Wise disclosed a system (see fig.137) for adaptive configuration, the system comprising:

adaptive configuration of an integrated circuit, the integrated circuit having first and second pluralities of heterogeneous computational elements (as newly amended on 08/09/07, see the adder and multiplier in fig.137) and an interconnection network, the interconnection network and the interconnection network having switching elements (see multiplexers in 137) , the method comprising:

receiving a first set of configuration information, the first set of configuration information comprising a first subset of configuration information and a second subset of configuration information (see carry-save multiplier , carry save adder, carry save subtractor and a second subset of configuration information : carry-save multiplier , carry save subtractor, carry save subtractor); using the routing elements (see multiplexers in fig.137) through the interconnection network, selectively routing data and the first subset of configuration information through the interconnection network to the first plurality of computational elements and the second subset of configuration information through the interconnection network to the second plurality of computational elements to provide a selected operating mode of a plurality of operating modes; in response to the first subset of configuration information, using the switching elements (multuiplexer) , configuring through the interconnection network the first plurality of computational elements for a first functional mode of a plurality of functional modes, the first plurality of computational elements having fixed and differing architectures (see x[2,5], x[3,4]);

in response to the second subset of configuration information (see carry-save multiplier , carry save subtractor, carry save subtractor in fig.137) using the switching elements

(multiplexer) , configuring through the interconnection network the second plurality of computational elements of the integrated circuit for a second, different functional mode of the plurality of functional modes (x[2,5] x[3,4]).
Wise also selectively routed his configuration information through the interconnection (see the multiplexed circuit configuration in fig.137). As the step for receiving and transmitting, see the input at x and output at the y bus.

As to the newly amended first level of interconnect network, Wise did not specifically show the first level of interconnection network as claimed. However, Brewer taught a switching network included multiple levels of routers or switches (see multistage routers in col.2, lines 14-27, col.8, lines 19-38 for two level hierarchy routers, see also col1. lines 5-15 for background teaching of the routers and switches). It would have been obvious to one of ordinary skill in the art to use Brewer in Wise for including the first level of interconnection network as claimed because the use of Brewer could provide Wise the ability to include deeper levels of interconnection network , thereby expanding the system interconnectivities, and because Wise also taught a memory map for mapping hardware resources into the memory address (see col.259, lines 10-25), and that his multiplexed network (see interconnection common box in fig.137) showed the points at which needed to be stored (see col.262, lines 14-20), which was recognizable by one of ordinary skill in the art that Wise's mapping of hardware resources were applicable for multilevel of the interconnect for purpose of higher level of network multiplexing.

As to claim 62, as to the heterogeneous computational elements, no specific type of heterogeneous computational elements has been reflected into the claim, therefore, it is read as any computational element with different function. See carry-save multiplier, carry save adder, carry save subtractor in the common block in fig.137.
As to claims 32, 63, Wise taught selectively switching the inputs and outputs (see inputs X and output Y in fig.137). Wise also taught receiving and transmitting configuration information (see the input at X and output at Y in fig.137). Wise did not specifically showed the selectively routing configuration to the plurality of the heterogeneous computational elements as claimed. However, Baxter taught selectively routing thought a network the configuration information (see the Interconnect Matrix in fig.1, see also the Interconnect Matrix for selectively routing in co1.10,, lines 26-38). It would have been obvious to one of ordinary skill in the art to use Baxter in Wise for including the selectively routing the first and second subset of configurations as claimed because the use of Baxter could provide Wise the capability to reconfigure the processing elements at a predefined set of selection, thereby increasing the flexibility of the configurations, and because Wise also taught his interconnection network (see the common box in i37 was a multiplexed circuit, see co1.262, lines 14-19), which was a suggestion of the applicability of the selective routing, and for the above reasons, provided motivation.

As to claims 33, 34, 64,65, Wise also included transmitting/receiving a first set of configuration information including a first subset of configuration information (see carry-save multiplier , carry save adder, carry save subtractor) and a second subset of configuration information (carry-save multiplier, carry save subtractor, carry save subtractor);

As to claims 35, 66, wise also taught the first set of configuration information corresponds to a first system reconfiguration capacity (see the y[3,2] x[3,4] connection path in fig.137) and the second set of configuration information corresponds to a second system reconfiguration capacity (see the y[7,6], x[2,5]).

As to claims 36, 67, see fig.137, co1.262, lines 14-20, see the multiplexed circuit.

As to claims 37-40,68-70, Wise also showed integrated circuit having a third plurality of heterogeneous elements (see subtractors and other components in fig.137) the storage of the configuration information in a memory (see the RAM organized into common control block in col.265, lines 43-53, see also the common control block in fig.137, for a machine-readable medium, see microprocessor read port in co1.260, lines 32-35, see RAM in co1.265, lines 43-53). See also teaching of Baxter and the reasoning of obviousness in the paragraph above.

As to claims 41,42,71 72,, Wise also taught the transmission through an air interface (carrier waves, see col.4, lines 21-23), and transmitted through a wireline interface (see telephone line in co1.4, lines 13-14.

47. As to claims 43,44, 73,74, Wise also taught configuration information embodied as a plurality of discrete information data packets, or a data team (see Discrete cosine transform in col.4, lines 1-11 for background, see also the data packet in coi.13, lines 53-57).

As to claims 45, 75, Wise also taught the first and second pluralities of heterogeneous computational elements comprise a plurality of fixed circuit architectures and plurality of fixed and different computational elements comprising a plurality of fixed architectures, the plurality of fixed circuit architectures comprising circuitry adapted to perform at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability (see memory, adder, multiplier, subtractor, input and output for field programmability, see dynamic adaptive configuration in col.6, lines 57-67, col.7, lines 1-12).

As to claims 46,76, Wise also included first and second function modes that comprises linear algorithmic operations (see co1.4, lines 8-9), non-linear algorithmic operations (see the transforms), finite state machine operations (see state machine stages in col.30, lines 62-67, co1.31, lines 1-4), controller operations, memory operations (see col.39, lines 35-57), and bit-level manipulations (see bit operation in col.40, lines 15-28), 50. As to claim 78, see Wise in the background taught carrier waves by a transmitter (see carrier waves, see co1.4, lines 21-23).

As to claim 48, Wise also included second d plurality of heterogeneous (heterogeneous as amended by applicant) elements configured for controller to direct and schedule the configuration of the first and second modes (see fig.137 adder and multiplier, see the clock control circuit at input in fig.141).

As to claim 49, Wise was also operative to time and schedule the configuration and reconfiguration of the plurality of heterogeneous computational elements with corresponding data (see the pipeline control of the algorithm and the control clock signals in co1.262, lines 55-65).

As to claim 51,52, Wise did not explicitly show the mobile station having a plurality of operating modes. However, Wise in the background taught carrier waves by a transmitter (see carrier waves, see col.4, lines 21-23). Therefore, Wise must have included a mobile station.

As to claims 53, 79, see servers in col.36, lines 14-19 in Baxter. 55. As to claims 54, 80, see the I/O T machines in fig.1.

As to claims 55, 85, Wise also taught request for configuration information (see the request in co1.64, lines 34-50).

As to claims 56,57, Wise also determined system reconfiguration capacity prior to utilizing the second set of configuration information to reconfigure for a second system operating mode (see the token information for reconfiguration in co1.61, lines 5-

22, see also the prediction filters to perform either filtering based on the token fig.17, co1.69, lines 11-20).

As to claim 62, Wise also taught a first portion of the plurality of heterogeneous computational elements (see configuration carry-save multiplier, carry save adder, carry save subtractor in the common block) are operating in the first functional mode (X[3,4]) while a second portion of the plurality of heterogeneous computational elements (see carry save multiplier, carry save subtractor, carry save subtractor) are being configured for the second functional mode (x[2,5])

As to claims 82-84, examiner holds that local area network and wide area net work were already known in the art.

Claims 16,19, 22, 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Brewer (5,519, 694) as applied to claims 1,17, 20, 23 above, and further in view of Lee et al. (5,873,045).

As to claims 24, 25, 26, limitations of parent claims have been discussed in previous paragraphs, therefore, it will not be repeated herein. Wise did not specifically show the personal digital assistance, multimedia reception, and paging as clamed. However, Lee disclosed personal digital assistance, multimedia reception, mobile packet-based communication (e.g. see col.3, lines 2-16). It would have been obvious to one of ordinary skill in the art to use Lee in wise for included the personal digital assistance, multimedia reception, and paging as clamed because the use of Lee could provide Wise

the ability to accept information from different type of devices(e.g., the cellular devices), and it could be done by predefine the mobile devices of Lee (e.g. the pager, personal assistant)' into the configuration file of Wise with modified control parameters (e.g. the R/VV format of the specific device) so that the specific mobile device of Lee could be recognized by Wise, and because Wise also taught carrier waves transmitter (see col. co1.4, lines 21-23), which was a suggestion of the demand for including e mobile devices (e.g. the pager, or personal assistant), as taught by Lee, into Wise in order to provide the enhanced capability of the system in Wise, and for doing so, provided a motivation.

As to claims 16,19,22, Wise did not specifically show the single bit stream of the configuration information as clamed. However, Lee disclosed a single bit stream of configuration information see the conversion into the single ended signal in col.8, lines 46-51). It would have been obvious to one of ordinary skill in the art to use Lee in Wise for including the single bit stream as claimed because the use of Lee could provide Wise the ability to adapt to different type of configuration information, therefore, increasing the capability of Wise to process a diverse set of configuration information, and Wise did disclose that his system was used for adapting to plurality of encoding standards (see co1.1, lines 60-67), which was an indication of the need for including the conversion of the multi-standard encoding signals into a single integrated format in order to reduce the hardware space of the system, and therefore, provided a motivation.

Claims 47,50, 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Brewer (5,519,694) and Baxter (5,794,062) in view, as applied to claims 32, 63, and further in view of Lee et al. (5,873,045).

As to claims 47,50,77, Wise , Brewer and Baxter did not specifically show the single bit stream of the configuration information as clamed. However, Lee disclosed a single bit stream of configuration information see the conversion into the single ended signal in col.8, lines 46-51). It would have been obvious to one of ordinary skill in the art to use Lee in Wise for including the single bit stream as claimed because the use of Lee could provide Wise the ability to adapt to different type of configuration information, therefore, increasing the capability of Wise to process a diverse set of configuration information, and Wise did disclose that his System was used for adapting to plurality of encoding standards (see co1.1, lines 60-67), which was an indication of the need for including the conversion of the multi-standard encoding signals into a single integrated format in order to reduce the hardware space of the system, and therefore, provided a motivation.

Claims 59, 61,86, 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise (5,768,561) in view of Brewer and Baxter (5,794,062) , as applied to claims 32,63, and further in view of Cohen et al. (6,005,943).

As to claims 59-61, 86-88, neither Wise nor Baxter nor Brewer specifically showed the decrypting the configuration, nor the authorization to receive the configuration as claimed. However, Cohen taught a decryptor and authorization of the configuration (see fig.2, col.8, lines 5-52). It would have been obvious to one of ordinary skill in the art to

use Cohen in Wise for including the decryption and authorization of the configuration as claimed because the use of Cohen could provide Wise the ability to accept the configuration information based on a predetermined set of requirements and restrictions, therefore increasing system security in Wise. Cohen is used to also show that decryption had been known in the art.

Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Webb (4,760,525) in view of Brewer (5,519, 694).

As to claim 63, Webb (4,760,525) taught at least:

a) Transmitting a first set of configuration information (see DATA2-DATA7 in fig.6), the first set of configuration information comprising a first subset of configuration information (DATA2, DATA3, DATA2, DATA4) and a second subset of configuration information (DATA5, DATA3, DATA6, DATA7); wherein when the first set of configuration information is received; using the routing elements (601,602), selectively routing data and the first subset of configuration information through the interconnection network (see fig.6) to the first plurality of computational elements (see ALU1 ALU2) and selectively routing data (see DATA) and the second subset of configuration information through the interconnection network to the second plurality of computational elements (ALU4 ALU3) to provide a selected operating mode of a plurality of operating modes; and using the switching elements (661,662), configuring through the second level of the an interconnection network the first plurality of fixed and differing computational

elements for a first functional mode (see the selection output odes RE1 RF and RG1 at MXB1 and MXB2 in fig.6) of a plurality of functional modes in response to the first subset of configuration information (see the selected input data at 661 and 662), and a second plurality of fixed and differing computational elements (ALU4 ALU3) for a second different functional mode (see output modes at RE1 RF and RG1 at MXB3 and MXB4) in response to the second subset of configuration information (see input data at 6631664).

Webb did not specifically show the first level and the second level as claimed. However, Brewer taught a switching network included multiple levels of routers or switches (see multistage routers in co1.2, lines 14-27, co1.8, lines 19-38 for two level hierarchy routers, see also co11. lines 5-15 for background teaching of the routers and Switches). It would have been obvious to one of ordinary skill in the art to use Brewer in Webb for including the first level and second level as claimed because the use of Brewer could provide Webb the control capability to interconnect higher level of network, and because Webb also taught configuring through the second level of the interconnection network including a plurality of fixed and differing computational elements for a plurality of functional modes in response to the first subset of configuration information (see the selection output odes RE1 RF and RG1 at MXB1 and MXB2 in fig.6, see the selected input data at 661 and 662) which was recognizable by one of ordinary skill in the art that Webb's second level of interconnect network would have required at least first level and second level of routing or switching devices for

interconnecting the multiplicity of computational elements, such as the one taught by Webb, and therefore, enhancing the interface hierarchy of the network elements.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Widergren et al. (4,302,775) is cited for the background teaching of the single bit stream configuration word with the respective function mode (e.g. see the single composite data stream in of the data with the col.23, lines 24-37).
b) Nosenchuck et al. (4,811,214) is cited for the teaching of the reconfigurable computational elements and memory for storing the configuration (see fig.2, fig.6m co1.7, lines 54-68, co1.8, lines 1-13).
c) Furuta et al. (6,281,703) is cited for the matrices of computational elements (see fig.4).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

/Daniel Pan/

Primary Examiner, Art Unit 2183